WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device, comprising:

a first step of implanting, into a channel formation region of a semiconductor substrate, first dopant ions of a first conductivity type which are heavy ions with a relatively large mass number to form a dopant implantation layer in the channel formation region; and

a second step of implanting second dopant ions into the semiconductor substrate to form an amorphous layer expanding from the substrate surface to a region of the substrate deeper than the dopant implantation layer.

2. The method of claim 1, wherein the semiconductor substrate is made of silicon, and the second dopant ion belongs to group IV elements.

3. The method of claim 2, wherein the plane orientation of the semiconductor substrate is the {100} plane.

4. The method of claim 2, wherein the semiconductor substrate includes, in the upper portion thereof, an epitaxial layer formed by epitaxially growing silicon.

5. The method of claim 2, wherein the semiconductor substrate includes, in the upper portion thereof, a strained silicon layer having a crystal lattice of a larger lattice constant than a normal lattice constant.

6. The method of claim 1, wherein the heavy ions are indium ions.

7. The method of claim 6, wherein the dose of the heavy ions to be implanted is 5×10^{13} /cm^2 or more.

8. The method of claim 1, further comprising, after the second step,

a third step of performing a first thermal treatment to diffuse the first dopant ions from the dopant implantation layer, thereby forming a first diffused layer of the first conductivity type in the channel formation region,

a fourth step of selectively forming a gate insulating film on the semiconductor substrate and a gate electrode on the gate insulating film,

a fifth step of implanting third dopant ions of a second conductivity type into the semiconductor substrate using the gate electrode as a mask, and

a sixth step of performing a second thermal treatment on the semiconductor substrate to diffuse the third dopant ions, thereby forming a second diffused layer of the second conductivity type whose junction position is relatively shallow.

9. The method of claim 8, wherein the first thermal treatment is rapid thermal annealing performed at a heating rate of about 100°C/sec or higher, at a heating temperature of 850 to 1050°C, and either with the peak temperature of the treatment kept for 10 seconds at the maximum or with the peak temperature not kept.

10. The method of claim 1, further comprising, between the second and third steps, the step of performing a third thermal treatment at such a temperature that the first dopant ions do not diffuse from the dopant implantation layer and that the crystallinity of the amorphous layer is restored, thereby recovering crystal damages caused by the first dopant ions.

11. The method of claim 10, wherein the heating temperature of the third thermal treatment is 400 to 600°C.

12. The method of claim 11, wherein the heating time of the third thermal treatment is 1 to 20 hours.

13. The method of claim 8, further comprising, between the fourth and sixth steps, the step of implanting fourth dopant ions of the first conductivity type into the semiconductor substrate using the gate electrode as a mask,

wherein the second thermal treatment performed in the sixth step diffuses the fourth dopant ions, thereby forming a third diffused layer of the first conductivity type below the second diffused layer.

14. The method of claim 8, further comprising, after the sixth step,

the step of forming sidewalls of an insulating film on the side surfaces of the gate electrode, and

the step of implanting fifth dopant ions of the second conductivity type into the semiconductor substrate using the gate electrode and the sidewalls as a mask and then performing a fourth thermal treatment to diffuse the fifth dopant ions, thereby forming, outside the second diffused layer, a fourth diffused layer of the second conductivity type which has a deeper junction interface than the second diffused layer.

15. A semiconductor device comprising:

a semiconductor substrate including a diffused channel layer in the upper portion thereof; and

a gate electrode formed above the semiconductor substrate with a gate insulating film interposed therebetween,

wherein the diffused channel layer is formed by implanting dopant ions which are heavy ions with a relatively large mass number, and the diffused channel layer contains germanium ions.

16. The device of claim 15, wherein germanium ions are contained also in a region of the semiconductor substrate located below the diffused channel layer.

17. The device of claim 15, wherein the heavy ions are indium ions.